CLAIM PTO

10/19/01

T.D.

CLAIM 1-11 (CANCELED)

12. An instruction sequence optimizing apparatus, for generating optimized code from an instruction sequence, comprising:

address assigning means for estimating a size of each instruction in the instruction sequence and assigning an address to each instruction, upper bits of each address indicating a memory address at which a processing packet is stored and lower bits of each address indicating a processing target instruction in the processing packet;

label detecting means

(1) for detecting a label, which should be resolved by an address of a specified instruction, from the instruction sequence, and obtaining the address of the specified instruction, and

(2) for detecting a label, which should be resolved by a difference in addresses of two specified instructions, from the instruction sequence, and obtaining the addresses of the two specified instructions;

program counter relative value calculating means for calculating, when a label which should be resolved by a difference in addresses of two specified instructions has been detected, a program counter relative value by subtracting an address of one of the two specified instructions from an address of another of the two specified instructions;

converting means

(1) for converting an instruction that has a label that should be resolved by an address of a specified instruction into an instruction with a size that is based on a size of the address of the specified instruction,

(2) for converting an instruction that has a label that should be resolved by a difference in addresses of two specified instructions into an instruction with a size that is based on a size of the program counter relative value calculated from the addresses of the two specified instructions; and

optimized code generating means for generating optimized code by converting addresses of instructions in accordance with the sizes of instructions after conversion by the converting means.

13. The instruction sequence optimizing apparatus of Claim 12,

wherein the program counter relative value calculating means includes a lower bit subtracting unit and an upper bit subtracting unit,

the lower bit subtracting unit subtracting lower bits of the address of the one of the two specified instructions from lower bits of the address of the other of the two specified instructions, for setting a result of a subtraction as lower bits of the program counter relative value, and sending any carry generated in the subtraction to the upper bit subtracting unit, and

the upper bit subtracting unit subtracting upper bits of the address of one of the two specified instructions and any carry received from the lower bit subtracting unit from upper bits of the address of the other of the two specified instructions, and for setting a result of a subtraction as upper bits of the program counter relative value.

14. The instruction sequence optimizing apparatus of Claim 12,

wherein the program counter relative value calculating means includes a lower bit subtracting unit and an upper bit subtracting unit,

the lower bit subtracting unit subtracting lower bits of the address of one of the two specified instructions from lower bits of the address of the other of the two specified instructions without generating a carry and setting a result of a subtraction as lower bits of the program counter relative value, and

the upper bit subtracting unit subtracting upper bits of the address of one of the two specified instructions from upper bits of the address of the other of the two specified instructions, and for setting a result of a subtraction as upper bits of the program counter relative value.

15. The instruction sequence optimizing apparatus of Claim 12,

wherein the program counter relative value calculating means subtracts upper bits of an address of one of the two specified instructions from upper bits of an address of the other of the two specified instructions, sets a result of a subtraction as upper bits of the program counter relative value, and sets lower bits of the other of the two specified instructions as lower bits of the program counter relative value.

16. An assembler that generates relocatable code from an instruction sequence, each address of an instruction in the instruction sequence having upper bits that indicate a memory address at which a processing packet is stored and lower bits that indicate a position of processing target instruction that is included in the processing packet,

the assembler comprising:

label detecting means for detecting a label in the instruction sequence that should be resolved by a difference in addresses between two specified instructions, and obtaining the addresses of the two specified instructions;

program counter relative value calculating means for calculating a program counter relative value by subtracting an address of one of the two specified instructions from an address of another of the two specified instructions; and

replacing means for replacing the label with the program counter relative value calculated by the program counter relative value calculating means.

17. The assembler of Claim 16,

wherein the program counter relative value calculating means includes a lower bit subtracting unit and an upper bit subtracting unit,

the lower bit subtracting unit subtracting lower bits of the address of the one of the two specified instructions from lower bits of the address of the other of the two specified instructions, for setting a result of a subtraction as lower bits of the program counter relative value, and sending any carry generated in the subtraction to the upper bit subtracting unit, and

the upper bit subtracting unit subtracting upper bits of the address of one of the two specified instructions and any carry received from the lower bit subtracting unit from upper bits of the address of the other of the two specified instructions, and for setting a result of a subtraction as upper bits of the program counter relative value.

18. The assembler of Claim 16,

wherein the program counter relative value calculating means includes a lower bit subtracting unit and an upper bit subtracting unit,

the lower bit subtracting unit subtracting lower bits of the address of one of the two specified instructions from lower bits of the address of the other of the two specified instructions without generating a carry and setting a result of a subtraction as lower bits of the program counter relative value, and

the upper bit subtracting unit subtracting upper bits of the address of one of the two specified instructions from upper bits of the address of the other of the two specified instructions, and for setting a result of a subtraction as upper bits of the program counter relative value.

19. The assembler of Claim 16,

wherein the program counter relative value calculating means subtracts upper bits of an address of one of the two specified instructions from upper bits of an address of the other of the two specified instructions, sets a result of a subtraction as upper bits of the program counter relative value, and sets lower bits of the other of the two specified instructions as lower bits of the program counter relative value.

20. A linker that generates object code by combining relocatable code, each address of an instruction in the relocatable code having upper bits that indicate a memory address at which a processing packet is stored and lower

bits that indicate a position of processing target instruction that is included in the processing packet,

the linker comprising:

relocation information detecting means for detecting a label in the relocatable code that should be resolved by a difference in addresses between two specified instructions, and obtaining the addresses of the two specified instructions;

program counter relative value calculating means for calculating a program counter relative value by subtracting an address of one of the two specified instructions from an address of another of the two specified instructions; and

replacing means for replacing the label with the program counter relative value calculated by the program counter relative value calculating means.

21. The linker of Claim 20,

wherein the program counter relative value calculating means includes a lower bit subtracting unit and an upper bit subtracting unit,

the lower bit subtracting unit subtracting lower bits of the address of the one of the two specified instructions from lower bits of the address of the other of the two specified instructions, for setting a result of a subtraction as lower bits of the program counter relative value, and sending any carry generated in the subtraction to the upper bit subtracting unit, and

the upper bit subtracting unit subtracting upper bits of the address of one of the two specified instructions and any carry received from the lower bit subtracting unit from upper bits of the address of the other of the two specified instructions, and for setting a result of a subtraction as upper bits of the program counter relative value.

22. The linker of Claim 20,

wherein the program counter relative value calculating means includes a lower bit subtracting unit and an upper bit subtracting unit,

the lower bit subtracting unit subtracting lower bits of the address of one of the two specified instructions from lower bits of the address of the other of the two specified instructions without generating a carry and setting a result of a subtraction as lower bits of the program counter relative value, and

the upper bit subtracting unit subtracting upper bits of the address of one of the two specified instructions from upper bits of the address of the other of the two specified instructions, and for setting a result of a subtraction as upper bits of the program counter relative value.

23. The linker of Claim 20,

wherein the program counter relative value calculating means subtracts upper bits of an address of one of the two specified instructions from upper bits of an address of the other of the two specified instructions, sets a result of a subtraction as upper bits of the program counter relative value, and sets lower bits of the other of the two specified instructions as lower bits of the program counter relative value.

24. A disassembler that receives an indication of an address of an instruction in object code and outputs an assembler name of the instruction at the indicated address, each address of an instruction in the object code having upper bits that indicate a memory address at which a processing packet is stored and lower bits that indicate a position of processing target instruction that is included in the processing packet,

the disassembler comprising:

program counter relative value extracting means for extracting, when the indicated instruction includes a program counter relative value, the program counter relative value from the indicated instruction;

label addressing calculating means for adding an address of the indicated instruction to the extracted program counter relative value and setting an addition result as a label address;

storing means for storing a label name corresponding to each label address; and

searching means for searching the storing means for a

label name that corresponds to the calculated label address and outputting the corresponding label name.

25. The disassembler of Claim 24,

wherein the label address calculating means includes a lower bit calculating unit and an upper bit calculating unit,

the lower bit calculating unit for adding lower bits of the address of the indicated instruction and lower bits of the program counter relative value, setting a result of an addition as lower bits of a label address, and sending any carry generated by the addition to the upper bit calculating unit, and

the upper bit calculating unit adding upper bits of the address of the indicated instruction, upper bits of the program counter relative value, and any carry received from the lower bit calculating unit, and setting a result of the an addition as upper bits of the label address.

26. The disassembler of Claim 24,

wherein the label address calculating means includes a lower bit calculating unit and an upper bit calculating unit,

the lower bit calculating unit adding lower bits of the address of the indicated instruction and lower bits of the program counter relative value without generating a carry, and setting a result of an addition as lower bits of

a label address, and

the upper bit calculating unit adding upper bits of the address of the indicated instruction and upper bits of the program counter relative value, and setting a result of an addition as upper bits of the label address.

27. The disassembler of Claim 24, wherein

the label address calculating means adds upper bits of the address of the indicated instruction and upper bits of the program counter relative value, sets a result of an addition as upper bits of the label address, and sets lower bits of the program counter relative value as lower bits of the label address.

CLAIMS 28-32 (CANCELED)

33. A computer-readable recording medium storing an

instruction sequence optimizing program that generates optimized code from an instruction sequence, the instruction sequence optimizing program including:

an address assigning step for estimating a size of each instruction in the instruction sequence and assigning an address to each instruction, upper bits of each address indicating a memory address at which a processing packet is stored and lower bits of each address indicating a processing target instruction in the processing packet;

a label detecting step (1) for detecting a label, which should be resolved by an address of a specified instruction, from the instruction sequence, and obtaining the address of the specified instruction, and

(2) for detecting a label, which should be resolved by a difference in addresses of two specified instructions, from the instruction sequence, and obtaining the addresses of the two specified instructions;

a program counter relative value calculating step for calculating, when a label which should be resolved by a difference in addresses of two specified instructions has been detected, a program counter relative value by subtracting an address of one of the two specified instructions from an address of another of the two specified instructions;

a converting step

(1) for converting an instruction that has a label that should be resolved by an address of a specified instruction into an instruction with a size that is based on a size of the address of the specified instruction,

(2) for converting an instruction that has a label that should be resolved by a difference in addresses of two specified instructions into an instruction with a size that is based on a size of the program counter relative value calculated from the addresses of the two specified instructions; and

an optimized code generating step for generating optimized code by converting addresses of instructions in accordance with the sizes of instructions after conversion in the converting step.

34. The computer-readable recording medium of Claim 33,

wherein the program counter relative value calculating step includes a lower bit subtracting substep and an upper bit subtracting substep,

the lower bit subtracting substep subtracting lower bits of the address of the one of the two specified instructions from lower bits of the address of the other of the two specified instructions, for setting a result of a subtraction as lower bits of the program counter relative value, and sending any carry generated in the subtraction to the upper bit subtracting substep, and

the upper bit subtracting substep subtracting upper

bits of the address of one of the two specified instructions and any carry received from the lower bit subtracting substep from upper bits of the address of the other of the two specified instructions, and for setting a result of a subtraction as upper bits of the program counter relative value.

35. The computer-readable recording medium of Claim 33,

wherein the program counter relative value calculating step includes a lower bit subtracting substep and an upper bit subtracting substep,

the lower bit subtracting substep subtracting lower bits of the address of one of the two specified instructions from lower bits of the address of the other of the two specified instructions without generating a carry and setting a result of a subtraction as lower bits of the program counter relative value, and

the upper bit subtracting substep subtracting upper bits of the address of one of the two specified instructions from upper bits of the address of the other of the two specified instructions, and for setting a result of a subtraction as upper bits of the program counter relative value.

36. The computer-readable recording medium of Claim 33,

wherein the program counter relative value calculating step subtracts upper bits of an address of one of the two specified instructions from upper bits of an address of the other of the two specified instructions, sets a result of a subtraction as upper bits of the program counter relative value, and sets lower bits of the other of the two specified instructions as lower bits of the program counter relative value.

37. A computer-readable recording medium storing an assembler program that generates relocatable code from optimized code that have been generated from an instruction sequence, each address of an instruction in the optimized code having upper bits that indicate a memory address at which a processing packet is stored and lower bits that indicate a position of processing target instruction that is included in the processing packet,

the assembler program comprising:

a label detecting step for detecting a label in the instruction sequence that should be resolved by a difference in addresses between two specified instructions, and obtaining the addresses of the two specified instructions;

a program counter relative value calculating step for calculating a program counter relative value by subtracting an address of one of the two specified instructions from an address of another of the two specified instructions; and

a replacing step for replacing the label with the program counter relative value calculated by the program

counter relative value calculating step.

38. The computer-readable recording medium of Claim 37,

wherein the program counter relative value calculating step includes a lower bit subtracting substep and an upper bit subtracting substep,

the lower bit subtracting substep subtracting lower bits of the address of the one of the two specified instructions from lower bits of the address of the other of the two specified instructions, for setting a result of a subtraction as lower bits of the program counter relative value, and sending any carry generated in the subtraction to the upper bit subtracting substep, and

the upper bit subtracting substep subtracting upper bits of the address of one of the two specified instructions and any carry received from the lower bit subtracting substep from upper bits of the address of the other of the two specified instructions, and for setting a result of a subtraction as upper bits of the program counter relative value.

39. The computer-readable recording medium of Claim 37,

wherein the program counter relative value calculating step includes a lower bit subtracting substep and an upper bit subtracting substep,

the lower bit subtracting substep subtracting lower bits of the address of one of the two specified

instructions from lower bits of the address of the other of the two specified instructions without generating a carry and setting a result of a subtraction as lower bits of the program counter relative value, and

the upper bit subtracting substep subtracting upper bits of the address of one of the two specified instructions from upper bits of the address of the other of the two specified instructions, and for setting a result of a subtraction as upper bits of the program counter relative value.

40. The computer-readable recording medium of Claim 37,

wherein the program counter relative value calculating step subtracts upper bits of an address of one of the two specified instructions from upper bits of an address of the other of the two specified instructions, sets a result of a subtraction as upper bits of the program counter relative value, and sets lower bits of the other of the two specified instructions as lower bits of the program counter relative value.

41. A computer-readable recording medium storing a linker program that generates object code from relocatable code that has been generated from an instruction sequence, each address of an instruction in the optimized code having upper bits that indicate a memory address at which a processing packet is stored and lower bits that indicate a

position of processing target instruction that is included in the processing packet,

the linker program comprising:

a relocation information detecting step for detecting a label in the relocatable code that should be resolved by a difference in addresses between two specified instructions, and obtaining the addresses of the two specified instructions;

a program counter relative value calculating step for calculating a program counter relative value by subtracting an address of one of the two specified instructions from an address of another of the two specified instructions; and

a replacing step for replacing the label with the program counter relative value calculated by the program counter relative value calculating step.

42. The computer-readable recording medium of Claim 41,

wherein the program counter relative value calculating step includes a lower bit subtracting substep and an upper bit subtracting substep,

the lower bit subtracting substep subtracting lower bits of the address of the one of the two specified instructions from lower bits of the address of the other of the two specified instructions, for setting a result of a subtraction as lower bits of the program counter relative value, and sending any carry generated in the subtraction to the upper bit subtracting substep, and

the upper bit subtracting substep subtracting upper bits of the address of one of the two specified instructions and any carry received from the lower bit subtracting substep from upper bits of the address of the other of the two specified instructions, and for setting a result of a subtraction as upper bits of the program counter relative value.

43. The computer-readable recording medium of Claim 41,

wherein the program counter relative value calculating step includes a lower bit subtracting substep and an upper bit subtracting substep,

the lower bit subtracting substep subtracting lower bits of the address of one of the two specified instructions from lower bits of the address of the other of the two specified instructions without generating a carry and setting a result of a subtraction as lower bits of the program counter relative value, and

the upper bit subtracting substep subtracting upper bits of the address of one of the two specified instructions from upper bits of the address of the other of the two specified instructions, and for setting a result of a subtraction as upper bits of the program counter relative value.

44. The computer-readable recording medium of Claim 41,

wherein the program counter relative value calculating step subtracts upper bits of an address of one of the two specified instructions from upper bits of an address of the other of the two specified instructions, sets a result of a subtraction as upper bits of the program counter relative value, and sets lower bits of the other of the two specified instructions as lower bits of the program counter relative value.

CLAIMS 45-48 (CANCELED)